APPLICATION NOTE

AN459
8XC750 watering controller

Peious Yoseph and Jean–Philippe Chevreau

1997 July 10

Philips
Semiconductors

PHILIPS

8XC750 watering controller AN459

Author: Peious Yoseph/Jean–Philippe Chevreau

INTRODUCTION

The 8XC750, as the lowest cost member of the Philips ’51 family, is uniquely suited for high-volume consumer application. At less than $2 in volume, the chip enables a wide variety of feature-rich, value-priced products. One example of such a design, a ’750 based watering controller (Figure 1), is described here.

The watering controller can handle many residential and commercial applications, thanks to a variety of fully programmable features. The unit controls up to eight zones (i.e., valves) with independent programs, start times (day of week, hour, minute) and durations (1–99 minutes) accommodating nearly any watering schedule.

The user interface, utilizing a high visibility 8-character alphanumeric display and four pushbuttons, is very easy to use. configuration is a simple matter of stepping through various menus and pushing INC or DEC pushbuttons (with auto-repeat) to set the desired value.

Beyond these basics, the controller incorporates a number of other options designed to enhance versatility and ease of use. Battery back-up with explicit battery status (LED) and outage (flashing ‘:’ in clock display) indicators insures the configuration is not lost during power failure. For at-a-glance status check, each zone has an activity LED that only illuminates if the valve is actually drawing power, easing diagnosis of cable and connection problems. Installation and service is further aided by a master valve power shutoff switch and status LED.

Finally, the design accommodates an optional external humidity sensor input. Should excessive humidity be detected (as during rainfall), a pending watering program is automatically skipped.

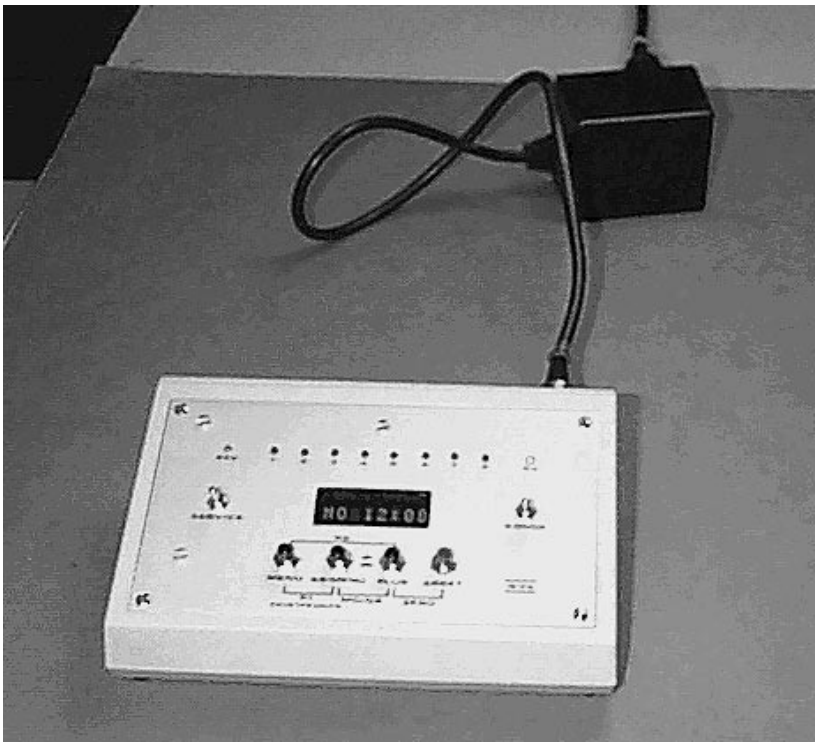
8XC750 OVERVIEW

The 8XC750 (Figure 2) uniquely combines excellent performance with the cost, power consumption, and form factor requirements of consumer applications. In particular, the ’750 represents the first step in a microprocessor upgrade path for previously mechanical, analog, and TTL-based controls.

Thanks to the powerful instructions set, the on-chip code (1KB EPROM) and data (64-byte RAM) space is more than able to accommodate the processing complexity required of simple control applications. Similarly, the 19 I/O lines are up to the task of interfacing with the variety of small displays and keypads that comprise the user interface for many products.

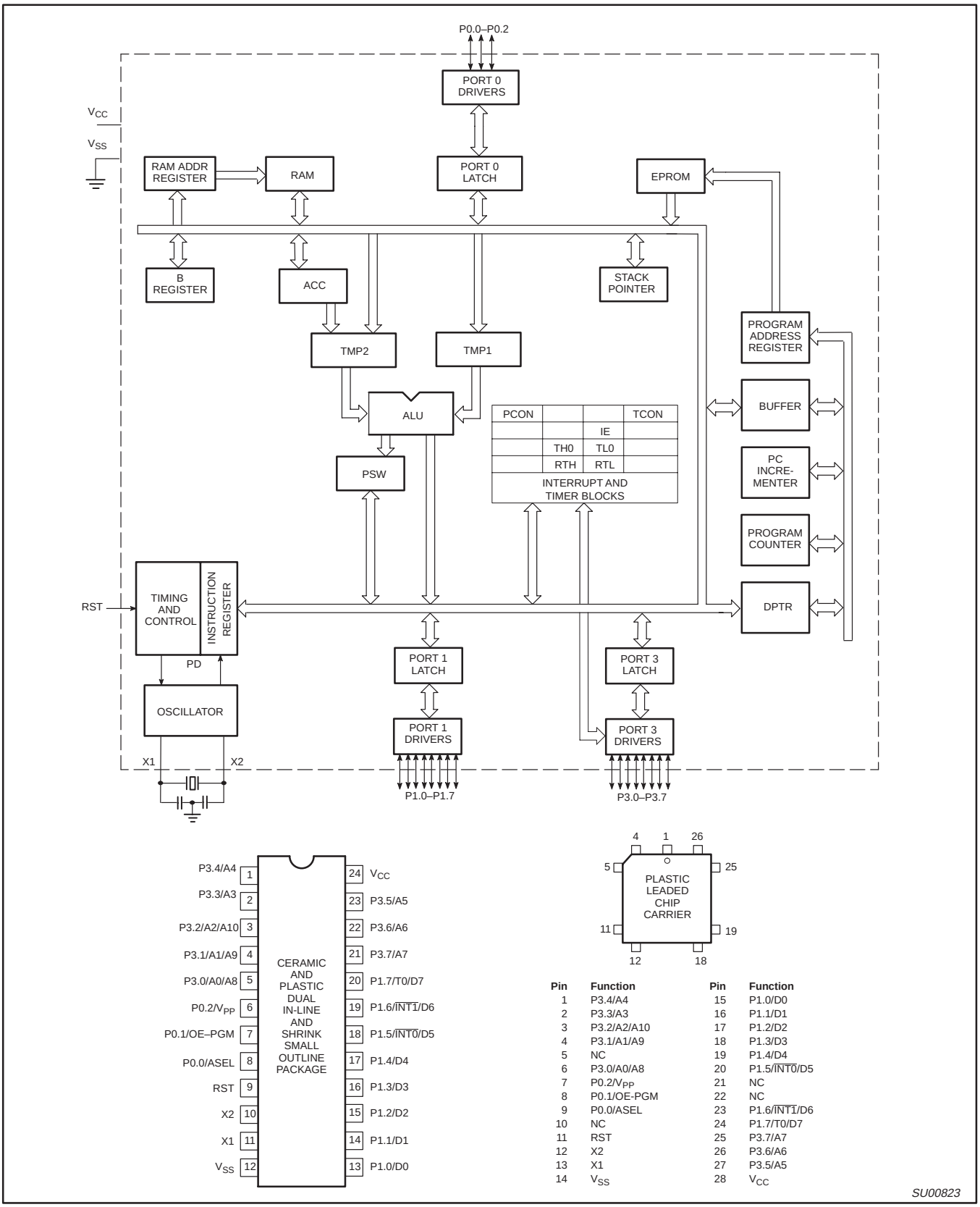
The ’750 streamlined design delivers benefits of particular significance for entry-level applications. Active power consumption is low (Figure 3) and two reduced power modes (IDLE and POWER DOWN) extend battery life while minimizing power supply and thermal management concerns. Small 24-pin “skinny-DIP” and 28-pin PLCC packages are joined by the truly tiny SSOP package (Figure 4) to reduce product size and weight, paramount in portable products.

Normally, such efficiency comes at the expense of performance, as in the case of 4-bit processors. Not so with the ’750, which, running at up to 40MHz, delivers multi-MIPS throughout. The on-chip 16-bit auto-reload timer and dual external interrupt inputs allow a ’750-based design to achieve sub-microsecond timing and control.



su00874

Figure 1. Watering Controller



Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	NC	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/$\overline{INT0}$/D5
7	P0.2/V_{PP}	21	NC
8	P0.1/OE-PGM	22	NC
9	P0.0/ASEL	23	P1.6/$\overline{INT1}$/D6
10	NC	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	V_{SS}	28	V_{CC}

Figure 2. ’750 Block Diagram

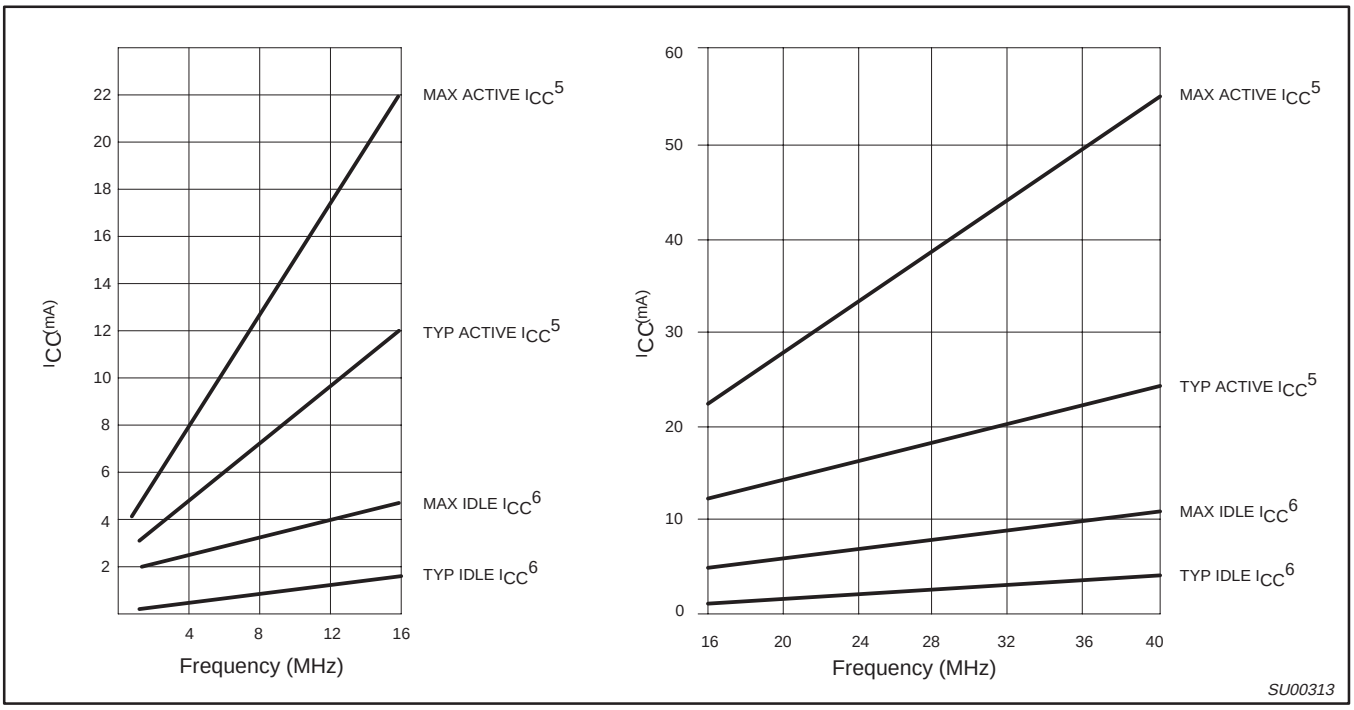
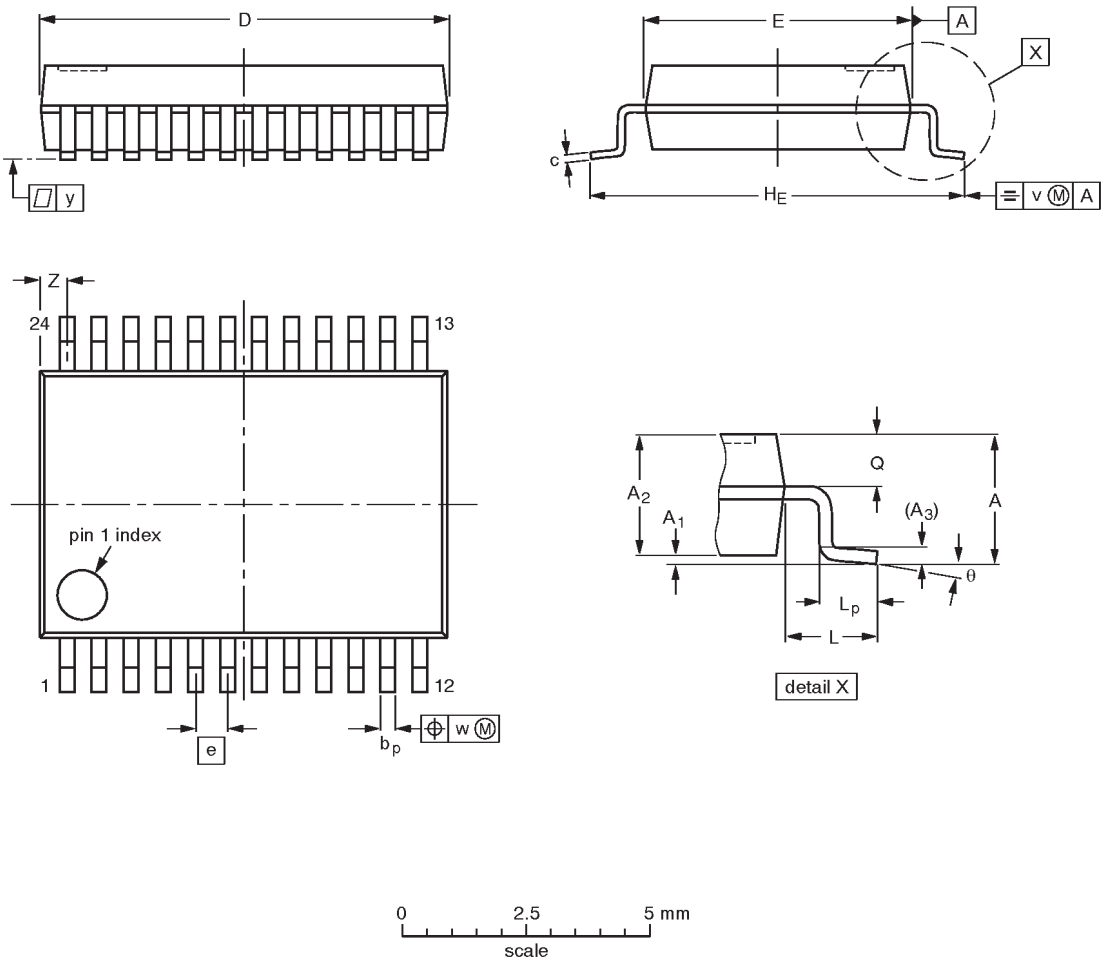


Figure 3. '750 Power Consumption
I_{CC} vs. Frequency
Maximum I_{CC}, values taken at V_{CC} max. and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0V and 25°C.
Notes 5 and 6 refer to *DC Electrical Characteristics* in the datasheet.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Figure 4. '750 SSOP Mechanical Drawing

WATERING CONTROLLER HARDWARE

The watering controller design has three functional blocks: CPU and front panel; power supply; and valve control (as shown in Figure 5). The first block encompasses the CPU, display, pushbuttons and TTL-compatible I/O. This portion of the design can be examined completely independent of real-world factors such as valve size, mains power, wiring and safety codes, etc.

The power supply (Figure 6) is responsible for generating +5V required by the CPU and front panel, as well as any other voltages (typically 24–30VAC, 28VAC in this example) required for valve control. The power section should also accommodate battery back-up by incorporating any necessary charging and switchover circuitry, as well as generating a Mains Power In (MPIN) signal to the CPU. In the example, MPIN is derived by dividing down the output (approximately +12V) from the center tap of the transformer. That output is also used in conjunction with a 12V relay to electrically isolate the humidity sensor input.

As shown in Figure 7, each valve control output from the CPU is AC coupled to a TRIAC. An LED monitors the output, and, as indicated earlier, is only illuminated when current actually flows through the valve.

Variance in geographic, regulatory and installation dependent factors does affect the power supply and valve control sections. Since a single ideal configuration cannot be predetermined, the circuits described above should only be considered examples that will likely require modification to best serve a particular application.

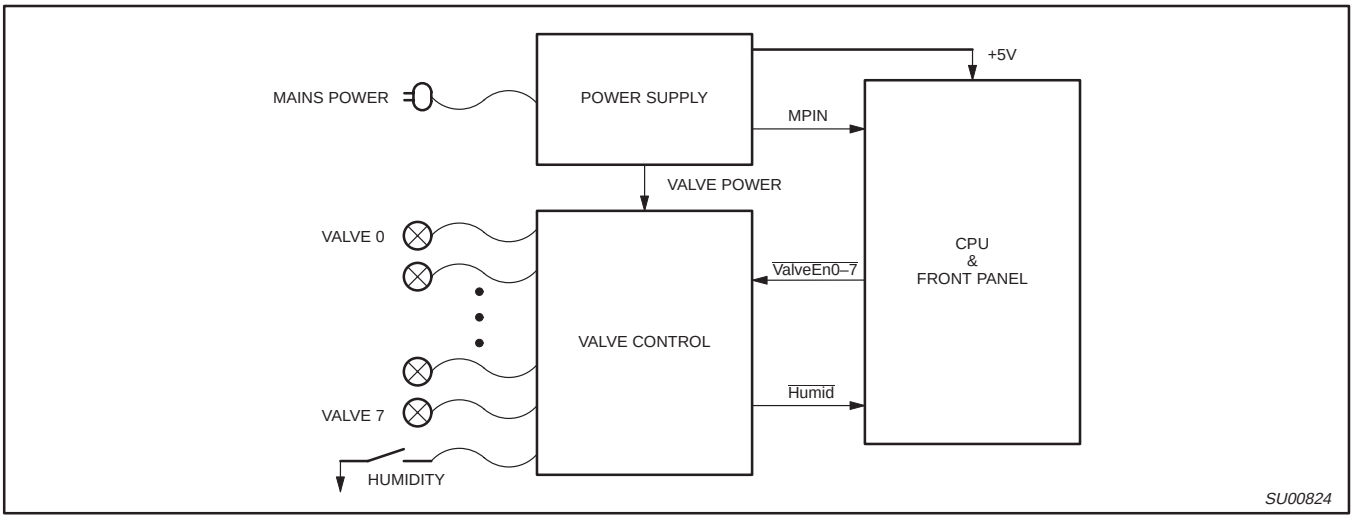


Figure 5. Watering Controller Block Diagram

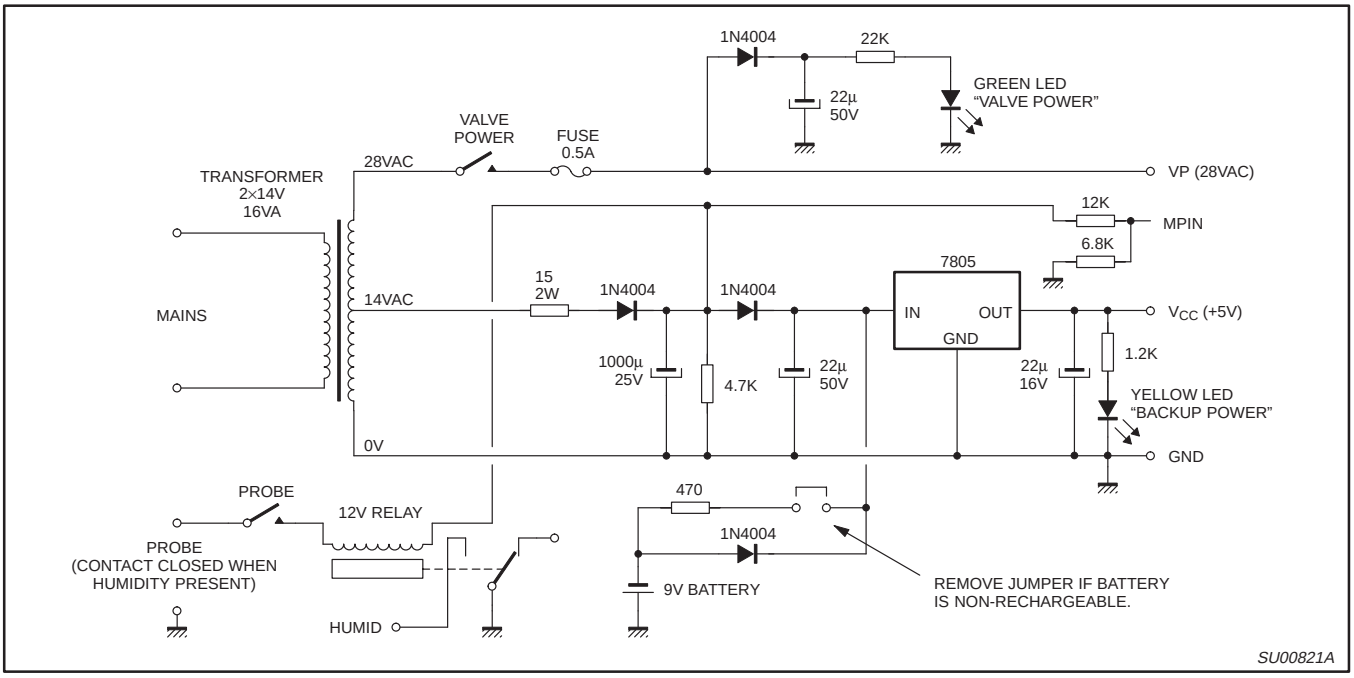


Figure 6. Power Supply Schematic

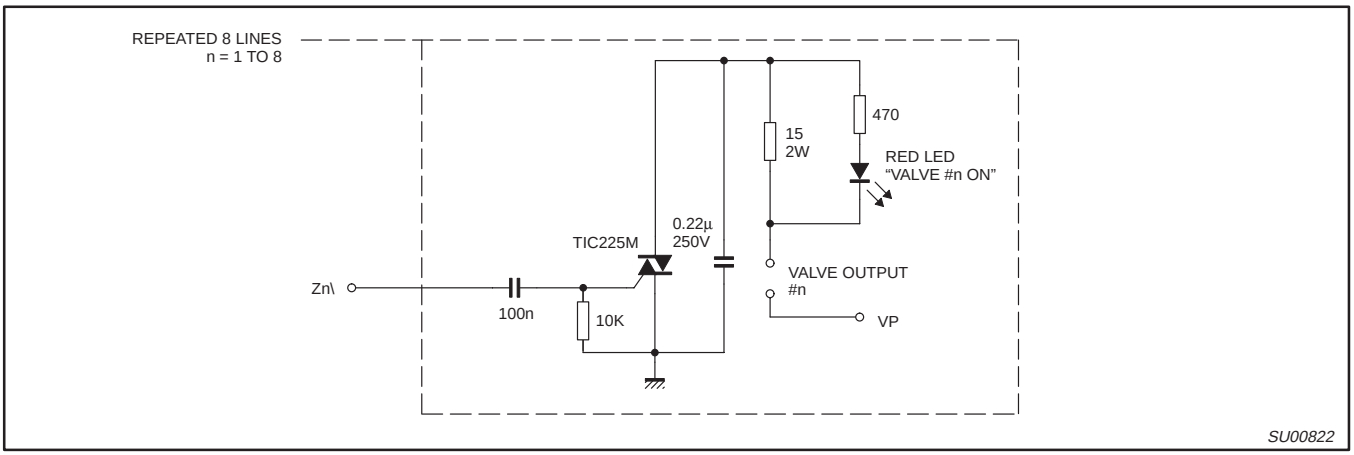


Figure 7. Valve Control Schematic

CPU AND FRONT PANEL

Unlike the power supply and valve control sections, this portion of the design (Figure 8) is quite universal. For instance, only the language used in menu prompts need be changed for worldwide adaptation.

P0.0 serves as the active LOW input from the humidity sensor, while the mains power detection input (MPIN, connected to P1.0) goes LOW to signal power failure. The CPU, presumed to continue to operate off battery power, responds by blanking the display to extend battery life.

Note that in this example the watering will stop, since mains power is required to activate the valves. However, the CPU continues to operate (i.e., keeping track of the current time and maintaining the stored schedule) until mains power is restored (MPIN goes HIGH), at which point the display is re-enabled and normal operation resumes automatically.

However, should the backup power source fail, the stored schedule will be lost. To accommodate this eventuality, a default watering schedule is loaded when power returns. A jumper (DEFIN—Default Schedule In—connected to P2.0) allows the user to choose whether to accept the default schedule or disable all watering until a new schedule is entered.

The valve selection is encoded on three bits (P1.0–1.2), and output via an 'HC138 3-to-8 line decoder. Only one valve can be turned on at any given time accommodating worst-case (i.e., low) water pressure applications. One gate input of the decoder is used to disable all outputs (i.e., watering off) and prevent glitches when switching between zones while another superimposes a free-running clock on the active output to prevent the TRIAC from switching off during zero-crossings.

Four pushbuttons are connected to the remaining bits (P1.4–1.7) of port 1 and are scanned and debounced in software. Internal pull-ups on the port pins eliminate the need for external resistors. A relatively long 120 ms debounce delay allows unambiguous detection of multiple simultaneous keypresses.

Port 3 connects to the display, a Hewlett-Packard HDSP-2111. Each of the eight character positions is comprised of a 5×7 LED matrix, offering excellent readability under all lighting conditions. The display includes built-in ASCII character generator and is available in a variety of colors (red, green, yellow). A plug-compatible unit, the HDSP-2511, with larger characters is also available (Figure 9).

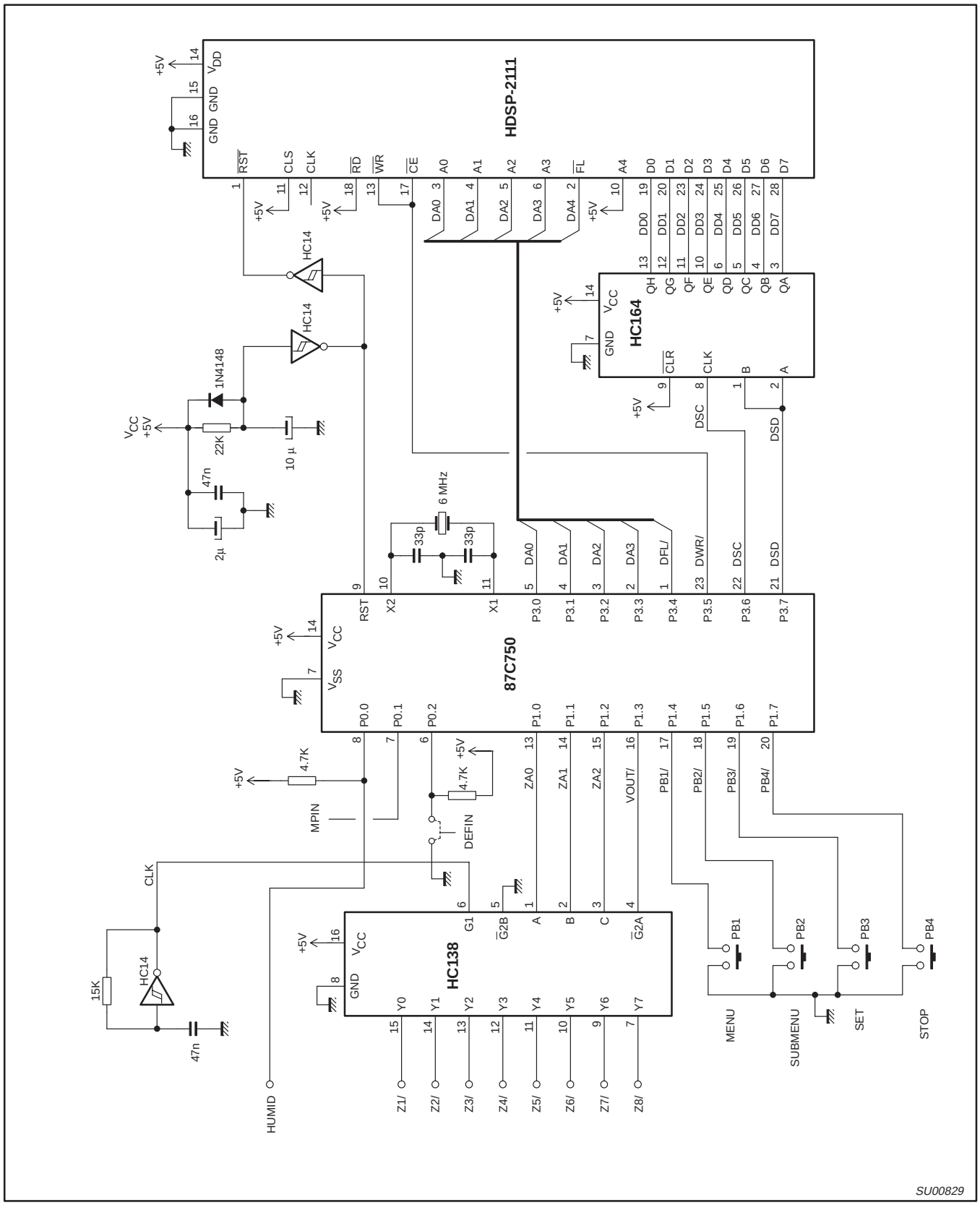


Figure 8. CPU and Front Panel Schematic

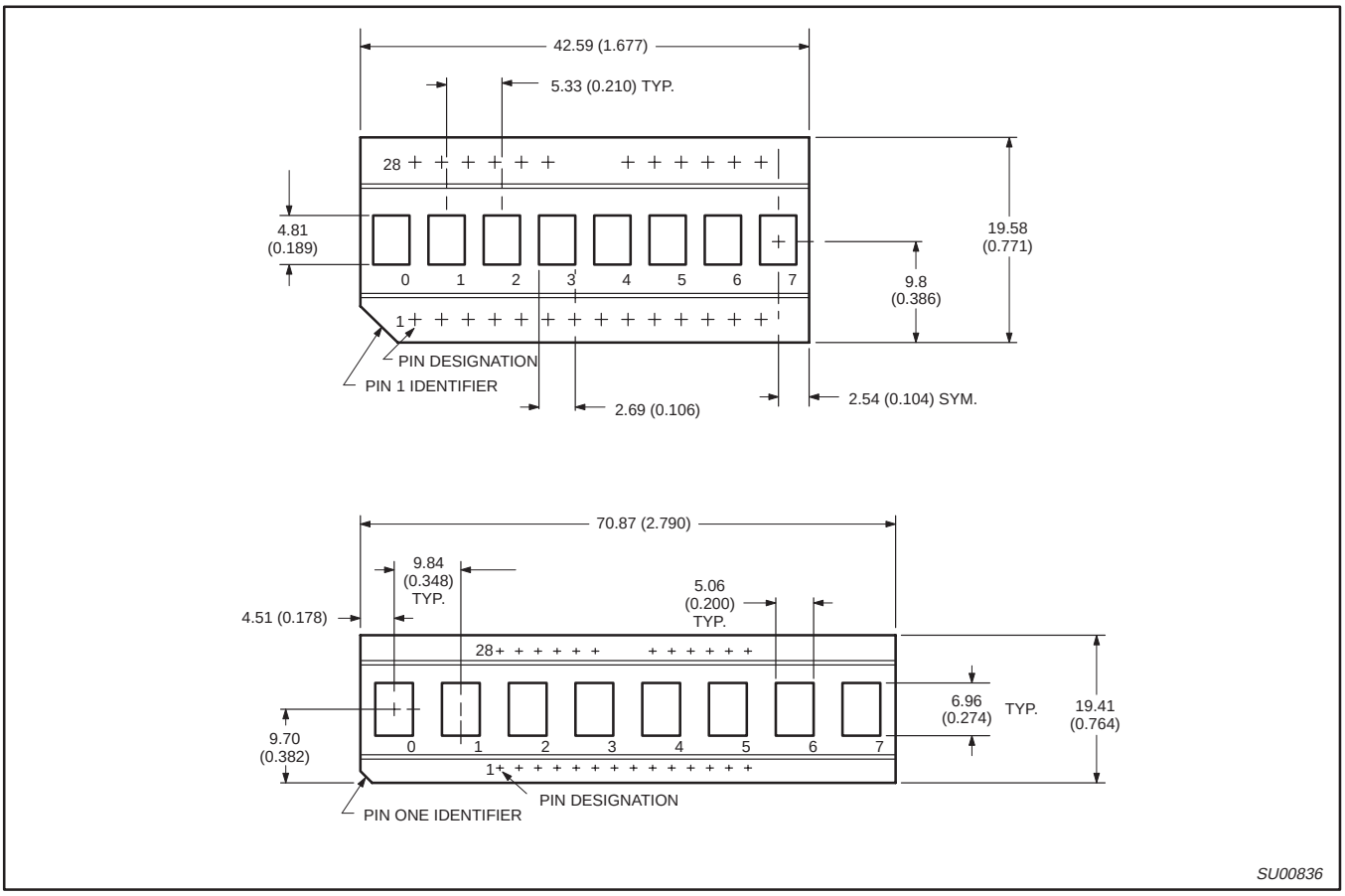


Figure 9. HP 2111 & 2511 Mechanical Drawing

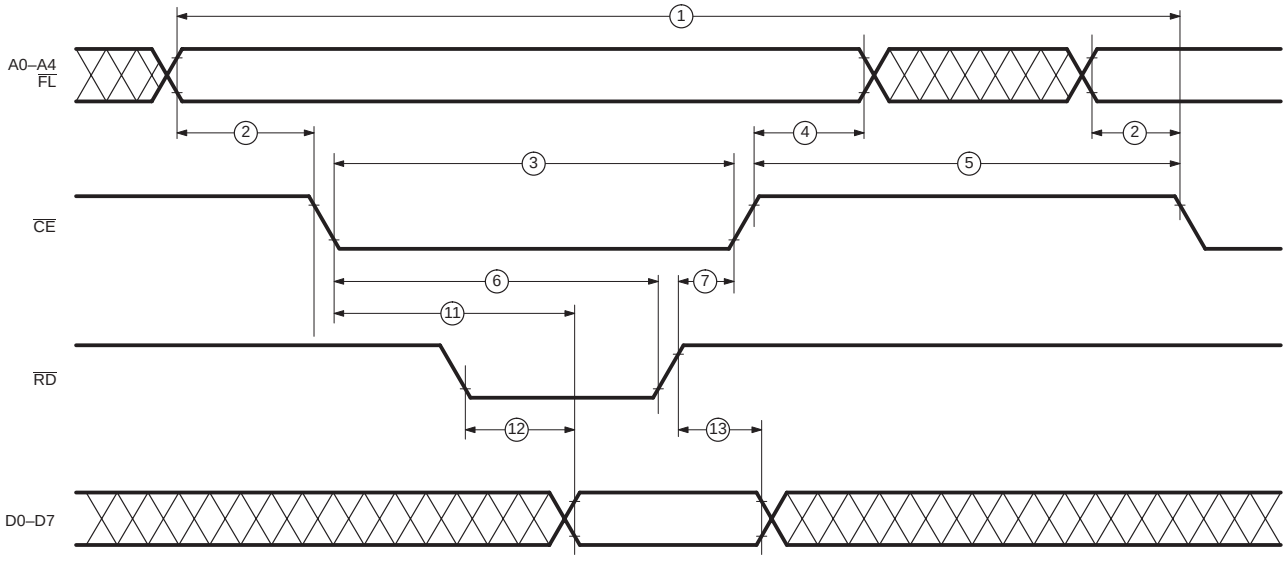
To accommodate the HDSP-2111 parallel interface (Figure 10), an 'HC164 shift register is used to expand two CPU outputs (P3.6 and 3.7) to an 8-bit data bus. Another output (P3.5) drives both the $\overline{WR}$ (Write) and $\overline{CE}$ (Chip Enable) inputs, a configuration allowed by the HDSP-2111 setup and hold timing specifications (Figure 11). The display $\overline{RD}$ (Read) line can simply be pulled up since reading of the display is not required in this application. The remaining bits of port 3 (P3.0–3.5) are connected to the display address bus comprised of A0–A3 and a $\overline{FL}$ (Flash) input. The latter is essentially an extra address line serving to access the blink attribute associated with the character position specified on A0–A2. As shown in Figure 12, A3 is also required in order to address the display control register, but A4 is simply pulled up since the UDC (User Defined Character) feature of the display is not used.

HDSP-2111 Pin Function Assignment Table

Pin No.	Function	Pin No.	Function
1	$\overline{RST}$	15	GND (Supply)
2	$\overline{FL}$	16	GND (Logic)
3	A0	17	$\overline{CE}$
4	A1	18	$\overline{RD}$
5	A2	19	D0
6	A3	20	D1
7	Do Not Connect	21	No Pin
8	Do Not Connect	22	No Pin
9	Do Not Connect	23	D2
10	A4	24	D3
11	CLS	25	D4
12	CLK	26	D5
13	$\overline{WR}$	27	D6
14	V_{DD}	28	D7

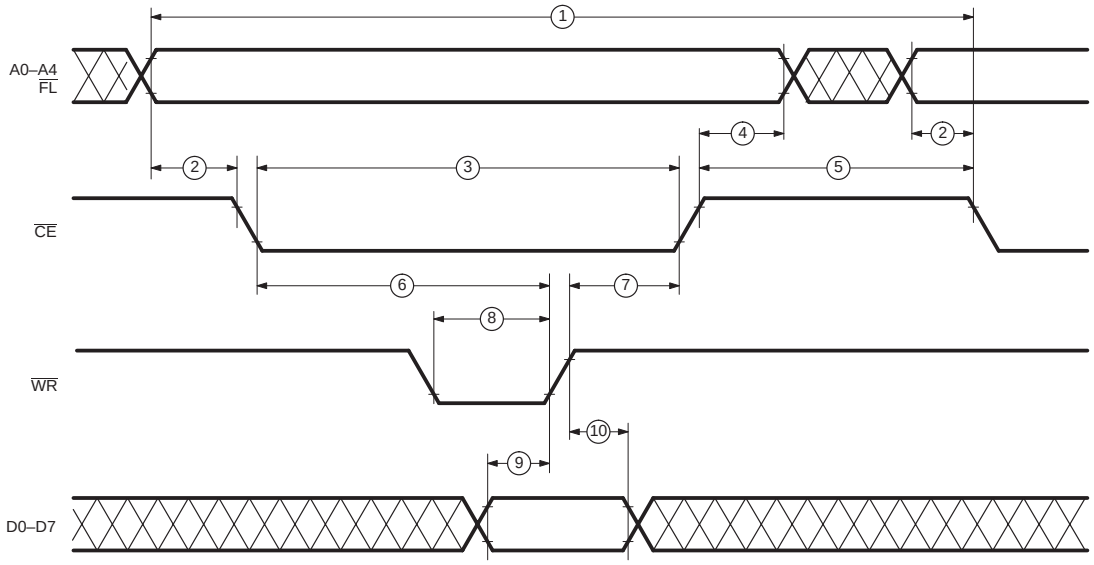
SU00826

Figure 10. HP 2111 Interface



INPUT PULSE LEVELS: 0.6V TO 2.4V
OUTPUT REFERENCE LEVELS: 0.6V TO 2.2V
OUTPUT LOADING = 1 TTL LOAD AND 100pFd

Read Cycle Timing Diagram



INPUT PULSE LEVELS – 0.8V TO 2.4V

Write Cycle Timing Diagram

SU00835

Figure 11. HP 2111 Timing Diagrams

AC TIMING CHARACTERISTICS

(Over temperature range –45°C to +85°C)
4.5V < V_{DD} < 5.5V, unless otherwise specified.

REFERENCE NUMBER	SYMBOL	DESCRIPTION	MIN.	UNITS
1	t_{ACC}	Display Access Time		
		Write	210	ns
		Read	230	ns
2	t_{ACS}	Address Setup Time to Chip Enable	10	
3	t_{CE}	Chip Enable Active Time		
		Write	140	ns
		Read	160	ns
4	t_{ACH}	Address Hold time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of		
		Write	140	ns
		Read	160	ns
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/Write Signal	0	ns
8	t_W	Write Active Time	100	ns
9	t_{WSU}	Data Write Setup Time	50	ns
10	t_{WH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time	300	ns

NOTES:
1. Worst case values occur at an IC junction temperature of 150°C.
2. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.
3. Changing the logic levels of the Address lines when $\overline{CE}$ = “0” may cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.
4. The display must not be accessed until after 3 clock pulses (110µs min. using the internal refresh clock) after the rising edge of the reset line.

Figure 11. HP 2111 Timing Diagram and Timing Characteristics (continued)

Section of Memory	$\overline{FL}$	A4	A3	A2, A1, A0
Flash RAM	0	X	X	Char. Address
UDC Address Register	1	0	0	Don’t Care
UDC RAM	1	0	1	Row Address
Control Word Register	1	1	0	Don’t Care
Character RAM	1	1	1	Character Address

SU00828

Figure 12. HP 2111 Address Map

Figure 13 shows the display control register. The brightness control bits are used to blank (i.e., 0% brightness) the display and reduce power consumption during mains outage. The flash bit is turned on to enable the character by character blink attribute function used when prompting for menu entries. The blink bit, which blinks all character positions synchronously, is asserted at power-up reset. Since power-up reset only occurs during initial installation or when battery back-up is lost during mains outage, a blinking display signals a schedule must be entered.

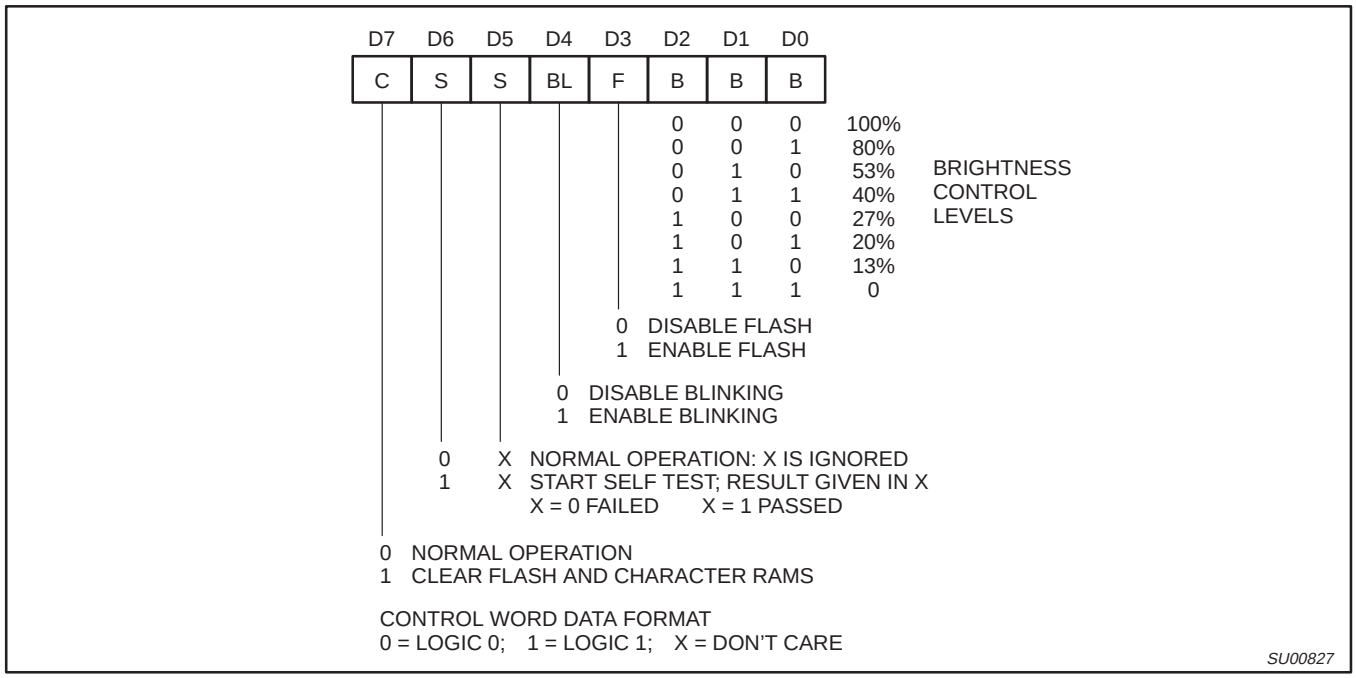


Figure 13. HP 2111 Display Control Register

WATERING CONTROLLER SOFTWARE

Though ‘C’ is an option (for example, see application note AN429: *Airflow measurement using the 83/87C752 and C*), assembly language is able to extract the most functionality from the ’750. Fortunately, the easy to understand instruction set, good code density and limited program size make assembly language a viable choice for ’750-based designs. This is especially true when unit hardware cost overshadows software development cost as is the case for high volume, cost sensitive consumer products.

Timing is derived from the 6.00 MHz crystal, generating a 2 microsecond timebase for the on-chip timer. The timer is initialized to generate an interrupt every 10 milliseconds, corresponding to 5000 (1388H) 2-microsecond periods by programming the reload registers (RTH and RTL) with EC78H (i.e., 10000H – 1388H).

The timer interrupt handler simply sets a GOT_TICK bit and returns. Actual updating of the real-time clock (i.e., wall clock and day of the week) variables is handled by a separate routine. This organization eliminates the need to stack registers (consuming valuable stack space) and allows other timing related functions, such as pushbutton debouncing, to exploit the high resolution (10 millisecond) timebase in a straightforward manner.

Note that crystals typically specify an accuracy of ±50 ppm which depends on temperature and design specific oscillator characteristics. Since the system may operate non-stop for years at a time, even a small error can accumulate to a noticeable degree. The CLOCK routine has the capability to digitally trim such errors by adding or subtracting hundredths of a second periodically. For example, if the error is 3 seconds/day, the second update can be skipped (or doubled) every 8 hours.

RAM allocation proves critical to fit all the required variables in the ’750 64-byte data space. A single register bank (8 bytes) provides all that’s needed for working storage. Careful analysis of subroutine call depth determines the maximum stack size of 10 bytes (i.e., PC stacking for 4-level call depth + timer interrupt). Four bytes store the current (real) time (day, hour, minute, second) and nearly half the RAM (31 bytes) is required to hold the scheduling info (dual program start times, durations for each zone and daily schedule). Times are stored in packed BCD format, taking advantage of the ’750 DA (Decimal Adjust) instruction. The ’750 bit handling capability is exploited by utilizing single–bit variables as much as possible.

One of the arts of embedded design is choosing the optimal tradeoff between program, data and hardware. for example, dedicating two RAM locations as surrogates for key HDSP-2111 registers (control and flash) makes the write-only interface possible, saving a pin.

Much of the program is devoted to handling the various data entry menus and prompts (Figure 13). However, final output to the display is via an OUT_CHAR subroutine that accepts the display address (character position) and data (ASCII value). Similarly, valve activation is handled with a subroutine that accepts a logical ZONE_NUM and the particular number of zones supported is defined as an EQUate. Thus, modifying the program to work with a different hardware design, such as a lower cost unit with fewer zones and an LCD display, is easy.

Figure 14 shows the water controller menus.

References:

For additional information, refer to HP Technical Data, HDSP–210X/–211X/–250X series of products at:

http://www.hp.com/HP–COMP/led_displays/hdsp210x.html

and you can find the full, PDF version of the data sheet at:

ftp://ftp.hp.com/pub/accesshp/HP–COMP/led_displays/hdsp210x.pdf

```
; 1.– In Menu Idle and in the Set Clock menu
;   ---------------------------------
;   | M | O |   | 1 | 2 | : | 0 | 0 |
;   ---------------------------------
;     Days        Hours      Minutes
;   Note: the clock display is on 24 hours (8 PM is displayed as 20:00).
;
; 2.– In the Set PR1 / PR2 Start Times menus
;   ---------------------------------
;   | P | 1 | A | 0 | 6 | : | 3 | 0 |
;   ---------------------------------
;    Program  ^      Start Time
;    Number   |  (Hours)     (Minutes)
;             |
;             \ (A or B)
;
; 3.– In the Set PR1 / PR2 Durations menus
;   ---------------------------------
;   | P | 1 |   | Z | 1 | : | 1 | 0 |
;   ---------------------------------
;    Program       Zone      Duration
;    Number       Number     (Minutes)
;
; 4.– In the Set Weekly Schedule menu
;   ---------------------------------
:   | M | O |   | P | 1 |   | – | – |
;   ---------------------------------
;     Days      Program #1  Program #2
;
;             Enabled: P1    Enabled: P2
;             Disabled: ––   Disabled: ––
;
; 5.– In the Test Sprinklers menu, before starting watering
;   ---------------------------------
;   | T | S |   | Z | 1 | : | 0 | 0 |
;   ---------------------------------
;     Test         Zone
;   Indicator     Number
;
; 6.– In the Test Sprinklers menu, after starting watering
;   ---------------------------------
;   | T | S |   | Z | 1 | : | 1 | 0 |
;   ---------------------------------
;     Test         Zone      Remaining
;   Indicator     Number     Duration
;                            (Minutes)
;
; 7.– When a Program is running
;   ---------------------------------
;   | P | 1 |   | Z | 1 | : | 1 | 0 |
;   ---------------------------------
;    Program       Zone      Remaining
;    Number       Number     Duration
;                            (Minutes)
```

SU00825

Figure 14. Water Controller Menus

NOTES

8XC750 watering controller AN459

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Let's make things better.

Philips Semiconductors

PHILIPS